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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,632	06/27/2003	Ana Luisa Lattes	42P16327	8372

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/608,632	LATTES, ANA LUISA
	Examiner	Art Unit
	Anh Q. Tran	2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,10,15-21,23-28,30 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,10,15-21,23-28,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 7, 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims recite "the second input to the predriver circuit is the same as the first input for the predriver circuit" is vague and indefinite. It is the same logic high/low signal or binary signal? Clarification is required.

3. Claims 4, 10, 18, 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims recites "the legs of the resistance network have a certain order and wherein the second input for each predriver circuit is an input for a leg of the resistance network matched in a reverse order" is vague and indefinite. How does the second input for each predriver ... matched in a reversed order? The second input is binary signal having only HIGH signal or LOW signal for turning ON/OFF passage, it doesn't have weight, resistance, or delay to match in reversed order. Also, the resistance network are in certain order is vague because in the specification the signals for turning ON/OFF the legs are in binary order, not the the legs arrangement.

An art rejection as best understood by the Examiner appear below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakata et al (6,838,914).

Sakata shows:

1. A driver comprising: a resistance network comprising a plurality of legs (IGBT1-IGBT6, Fig. 13); and a plurality of predriver circuits (each of the leg IGBT is control by a corresponding one of Driver Control Circuit 1 shown in figure 2, col. 4, lines 25-30), each of the plurality of predriver circuits being associated with one of the plurality of legs of the resistance network, each predriver circuit to receive a first input (Upin, Fig. 2) to determine whether the predriver produces a signal and a second input (d1-d6) to determine when to produce the signal, each of the plurality of predriver circuits comprising a passgate (S1-S6 are transistors) and a capacitor (C1-C6).

2. the driver of claim 1, wherein the first input indicates whether the associated leg of the resistance network is active (Upin to Activate or deactivate IGBT1, Fig. 1).

3. the driver of claim 2, wherein the second input to the predriver circuit either is the same as the first input for the predriver circuit or is the first input for another of the predriver circuits (d1-d6 are control signals for all Driver Controlller).

4. The driver of claim 3, wherein the legs of the resistance network are in a certain order and wherein the second input for each predriver circuit is an input for a leg of the resistance network matched in a reversed order (S1-S6 can be selected in any order by d1-d6).

5. The driver of claim 3, wherein if a predriver circuit produces a signal:

the predriver circuit produces the signal after a first time interval (tonP, col. 4, lines 38-44) if the second input to the predriver circuit indicates that the relevant leg is active, and the predriver circuit produces after a second time interval (toffP, col. 4, lines 45-51) if the second input to the predriver circuit indicates that the relevant leg is inactive.

6. The driver of claim 5, wherein slower conditions result in more active legs producing signals using a shorter time interval (S1-S6 and C1-C6 are delay elements which are selectable by d1-d6, slower conditions is when S1-S6 is OFF).

7. The driver of claim 5, wherein faster conditions result in more of the legs that are active producing signals using a longer time interval (faster conditions is when S1-S6 is ON).

9. The driver of claim 1, wherein the second input to the predriver circuit is applied to the passgate, the second input determining whether the passgate opens or closes a path to the capacitor.

10. the limitations of claim 10 is rejected as above.

15. A device comprising:

an interface (Fig. 13) to a bus (Line Output); and

an I/O driver circuit (Driver Controller Circuit and IGBT1-IGBT6) signals on the bus, the I/O driver comprising: (the rest of limitations are rejected as above).

16-19, 23. the limitations are rejected as above.

20. The device of claim 19, wherein if PVT (process, voltage, or temperature) conditions for the device result in slower operation, more of the active predriver circuits produce signals after a shorter delay (S1-S6 are OFF).

21. The device of claim 20, wherein if PVT conditions for the device result in faster operation, more of the active predriver circuits produce signals after a longer delay (S1-S6 are ON).

24. A system comprising: a processor (MCU); a bus (Line Ouput),

a driver to drive signals on the bus, the driver comprising: (the rest of the limitations are rejected as above.

25-28. the claimed are rejected as above claims.

30-31. The apparatus described above is applicable to the method claims.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee (6,256,235).

Lee shows:

30. A method comprising: receiving a first input and a second input for each of a plurality of signals, wherein:

the first input (TRI-A to TRI-C) for each of the plurality of signals indicates whether a resistance associated with the signal is active, the resistance comprising one leg of a resistance network, the resistance network comprising a plurality of legs (23A – 23C), and the second input (EN_AP and EN_AN to EN_CP and EN_CN) indicates whether one leg of the plurality of legs of the resistance network is active; determining whether to produce each signal based at least in part on the first input for the signal; and

determining when to produce each signal based at least in part on the second input for the signal, wherein determining when to produce each signal comprises choosing to produce a signal after a first delay (e.g., 33B and 33A is ON, both delaying the signal) if the second input for the signal is active and choosing to produce the signal after a second delay if the second input for the signal is inactive (e.g., inverters 33A is OFF, only 33B is delaying the signal).

30. A method comprising: receiving a first input and a second input for each of a plurality of signals, wherein:

the first input (TRI-A to TRI-C) for each of the plurality of signals indicates whether a resistance associated with the signal is active, the resistance comprising one leg of a resistance network, the resistance network comprising a plurality of legs (23A – 23C), and the second input (EN_AP and EN_AN to EN_CP and EN_CN) indicates whether one leg of the plurality of legs of the resistance network is active;

determining whether to produce each signal based at least in part on the first input for the signal; and determining when to produce each signal based at least in part on the second input for the signal, wherein determining when to produce each signal comprises choosing to produce the signal after a shorter delay (e.g., inverters 33A is OFF, only 33B is delaying the signal) in slow conditions and choosing to produce the signal after a longer delay (e.g., 33B and 33A is ON, both delaying the signal) in fast conditions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

10/5/05